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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,492	07/16/2003	Majid Movahed Mansoori	TI-35375	9069

23494 7590 04/04/2006

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EXAMINER	
LINDSAY JR, WALTER LEE	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 04/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,492	MANSOORI ET AL.	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,2,4-14,20 and 22-26* is/are allowed.

6)☒ Claim(s) *15-19,27 and 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an RCE filed on 2/09/2006.

Currently, claims 1-2 and 4-28 are pending.

Specification

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 15, 21, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dokumaci (U.S. Patent No. 6,686,637, filed 11/21/2002) in view of Sagnes (U.S. Patent No. 5,998,289, dated 12/7/1999).

Dokumaci shows the method substantially as claimed, in Figs. 1-12 and corresponding text as: forming a layer of dielectric material (104) over a substrate (106) (Fig. 1) (col. 3, lines 6-19); forming a layer of poly-SiGe with carbon (102) over a dielectric layer situated on the substrate (Fig. 1) (col. 3, lines 6-19) (col. 4, lines 47-55); forming a layer of poly-Si (116) over the layer of poly-SiGe (Fig. 6) (col. 3, line 62-col. 4, line 10); patterning the poly-Si (118), poly-SiGe (110) and dielectric layer to form a gate stack (Fig. 10) (col. 4, lines 23-34); and doping exposed portions of the substrate adjacent to the gate stack to form source and drain regions (126) (Fig. 11) (col. 4, lines 11-23) (claim 15). Dokumaci teaches that in the layer of poly-Si includes carbon (Fig. 11)(col. 4, lines 23-34) (claim 21)[carbon is implanted into 118].

Dokumaci lacks anticipation only in not explicitly teaching that: 1) the poly-Si, poly-SiGe and dielectric layers are patterned and etched to form a gate stack (claim 15); 2) the poly-SiGe layer has a thickness of about 400 to 700 Angstroms (claim 27); and 3) the poly-Si layer has a thickness of about 350 to 750 Angstroms (claim 28).

Sagnes teaches a silicon-germanium gate transistor. Sagnes shows a gate stack formed by plasma etch (col. 8, lines 5-10). Sagnes shows the polycrystalline $Si_{1-x}Ge_x$ layer having a thickness between 50nm (500 Angstroms) and 200 nm (2000 Angstroms) and thickness of polycrystalline Si is between 50nm (500 Angstroms) to 150nm (1500 Angstroms) (col. 3, lines 13-21). The SiGe material, has a lower resistance than polycrystalline silicon, offers the possibility of shifting the threshold voltage of a PMOS and can act as a mid-gap material.

Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See In re Aller, Lacey and Hall (10 USPQ 233-237) It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 f.2d 1575,1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

It would be obvious to one of ordinary skill in the art, at the time the invention was made to modify, the method shown in Dokumaci, where a poly-SiGe layer has a thickness of about 400 to 700 Angstroms and that the poly-Si layer has a thickness of about 350 to 750 Angstroms, as taught by Sagnes, with the motivation that Sagnes teaches that SiGe material has a lower resistance than polycrystalline silicon, offers the possibility of shifting the threshold voltage of a PMOS and can act as a mid-gap material.

5. Claims 16-19 are rejected under 35 U.S.C. 103(a) as being obvious over Dokumaci et al. (U.S. Patent No. 6,686,637 filed 11/21/2002) in view of Moslehi (U.S. Patent No. 5,397,909 dated 3/14/1995).

Dokumaci shows the method substantially as claimed and as described in the preceding paragraphs.

Dokumaci shows the method substantially as claimed, in Figs. 1-12 and corresponding text and, as previously described including: doping exposed regions of the substrate adjacent the gate stack to form source and drain extension regions (120) before forming the source and drain regions (Fig. 10) (col. 4, lines 11-23) (claim 16). Dokumaci teaches forming sidewall spacers (124) adjacent the gate structure prior to forming the source and drain regions (126), but after forming the source and drain extension regions (Fig. 11) (col. 4, lines 11-23) (claim 17).

Dokumaci lacks anticipation only in not explicitly teaching that: 1) the source and drain extension regions are lightly doped relative to the source and drain regions (claim 16); 2) a layer of insulating material is formed over the gate stack and exposed portions of the substrate; and selectively removing portions of the insulating material (claim 18); and 3) the insulating material comprises at least one of silicon nitride and silicon oxide (claim 19).

Moslehi teaches a MOSFET device that employs a double gate, and a lightly doped source drain region. Moslehi forms a dielectric layer (48) on the order of 100 Angstroms (col. 11, lines 25-28) and implants source/drain lightly doped extension region (58) through the dielectric layer before the formation of sidewall spacer (60) (col. 12, lines 41-68). Sidewall spacers (60) are formed by depositing silicon nitride or silicon oxide over the substrate and gate, etching the insulating layer to form the spacers (col. 12, line 67-col. 13, line 20). Additionally the source/drain region (64) is formed to complete the device (col. 13, lines 31-45). The process described by Moslehi lends itself to both p or n-channel devices, it also provides for reduced device punch-through

leakage and to reduce degradation of process control due to changes in threshold voltage.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify the method shown in Dokumaci so that the dielectric layer has a thickness of about 100 Angstroms, the source and drain extension regions are lightly doped relative to the source and drain regions, and forming a layer of insulating material over the gate stack and exposed portions of the substrate and selectively removing portions of the insulating material, the insulating material being either silicon nitride or silicon oxide, as taught by Moslehi, with the motivation that Moslehi teaches that both p or n-channel devices can be formed, that a reduction of punch-through leakage is achieved and that degradation of process control due to changes in threshold voltage are reduced.

Allowable Subject Matter

1. Claims 1, 2, 4-14 and 20, 22-26 are allowed.

2. The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...forming a polysilicon seed layer over the dielectric layer;

forming a layer of poly-Si over the layer of poly-SiGe; and

patterning the poly-Si, poly-SiGe and dielectric layers to form the gate stack, wherein the polysilicon seed layer is patterned in forming the gate stack, as required by claim 1;

...forming a polysilicon seed layer over the layer of dielectric material, as required by claim 20; and

...wherein the seed layer over the dielectric layer, as required by claim 22.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL
March 30, 2006